coupling a probe card to the semiconductor wafer through a plurality of probe needles on said probe card corresponding to said plurality of external terminals of each of said integrated circuit chips, said probe card receiving a plurality of independent test signals and a power supply signal from a tester, wherein said probe card includes structure defining a rectangular through hole having first and second long sides, and wherein the probe needles extend through the rectangular through hole;

concurrently supplying the independent test signals and the power supply signal from the tester through the probe needles to said plurality of external terminals of said plurality of integrated circuits; and

concurrently measuring electric characteristics of said semiconductor integrated circuit chips in an independent manner.

7. (Amended) The method of claim 6, wherein said external terminals are centrally disposed within said integrated circuit chips, with integrated circuits on either side of said external terminals.

8. (Amended) The method of claim 7, wherein said external terminals are arranged in a plurality of columns and rows.

9. (Amended) The method of claim 8, wherein the step of providing a semiconductor wafer includes forming memory arrays for each of said integrated circuit chips.

10. (Amended) The method of claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on internal layers of said probe card.

\\\LA - 81790/0189 - 1G1651 v2
Received from < 12133376701 > at 4/10/03 9:23:45 PM [Eastern Daylight Time]

11. (Amended) The method of claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on different internal layers of said probe card, said wiring lines positioned on different ones of said different internal layers according to a type of signal carried by said wiring lines.

12. (Amended) A probing test method of semiconductor integrated circuits, comprising:

preparing at least one semiconductor wafer, said semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged thereon in rows and columns, said semiconductor integrated circuit chips having a plurality of external pads;

preparing at least one probe card, said probe card having a plurality of connection terminals for receiving from a tester a test signal and a power supply signal, said at least one probe card having a plurality of probe needles corresponding to said plurality of external pads, respectively, wherein said probe card includes structure defining a rectangular through hole having first and second long sides, and wherein the probe needles extend through the rectangular through hole;

supplying said test signal and said power supply signal from said tester to said probe needles by way of said connection terminals in a completely independent manner;

supplying said test signal and said power supply signal from said probe needles to said semiconductor integrated circuit chips, by way of said external pads, in a completely independent and concurrent manner; and

\\\LA - 81790/0189 - 161551 v2
Received from < 12133376701 > at 4/10/03 9:23:45 PM [Eastern Daylight Time]

measuring electric characteristics of the semiconductor integrated circuit chips in a completely independent and concurrent manner.

\\\LA - 81790/0183 - 161551 v2
Received from < 12133376701 > at 4/10/03 9:23:45 PM [Eastern Daylight Time]